

CLAIMS

1. A method of forming a semiconductor package comprising:
- 5 encapsulating a plurality of package sites that are on a substrate wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites; and
- singulating through the encapsulating material to
- 10 singulate each package site.
2. The method of claim 1 wherein encapsulating the plurality of package sites includes forming the encapsulating material to have a top surface planarity
- 15 deviation of less than 0.13 millimeters.
3. The method of claim 1 wherein encapsulating the plurality of package sites includes forming a dam bar surrounding the periphery of the plurality of package
- 20 sites for forming a cavity containing the plurality of package sites, and dispensing the encapsulating material within the cavity.
4. The method of claim 3 wherein forming the dam
- 25 bar includes dispensing a first encapsulating material having a first viscosity.
5. The method of claim 4 wherein dispensing the encapsulating material within the cavity includes
- 30 dispensing a second encapsulating material having a second viscosity that is lower than the first viscosity.

6. The method of claim 5 wherein dispensing the first encapsulating material having the first viscosity includes having a viscosity of 1,000,000 to 2,000,000 cps.

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7. The method of claim 5 wherein dispensing the second encapsulating material having the second viscosity includes having a viscosity less than 500,000 cps.

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8. The method of claim 5 further including gelling both the first and second encapsulating materials prior to curing both the first and second encapsulating materials.

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9. The method of claim 5 wherein dispensing the first encapsulating material includes heating the first encapsulating material.

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10. The method of claim 5 wherein dispensing the second encapsulating material includes heating the second encapsulating material.

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11. The method of claim 1 wherein singulating through the encapsulating material includes sawing through the encapsulating material and the substrate.

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12. The method of claim 1 wherein encapsulating the plurality of package sites includes encapsulating by overmolding.

13. A semiconductor package comprising:

an interconnect substrate having a plurality of package sites wherein each package site of the plurality of package sites is substantially similar and can be

5 singulated from the substrate;

a dam bar surrounding the plurality of package sites for forming a cavity wherein the plurality of package sites are in the cavity; and

an encapsulant filling the cavity, the encapsulant
10 having a top surface planarity deviation of less than
0.13 millimeters.